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10/729,095	12/05/2003	Chih-Hsin Ko	TSM03-0615	8817

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EXAMINER	
VU, HUNG K	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 07/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/729,095	KO ET AL.
	Examiner	Art Unit
	Hung Vu	2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17-103* is/are pending in the application.

4a) Of the above claim(s) *21-23,25,34,36,37,78,79,83 and 88-103* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17-20,24,26-33,35,38-77,80-82 and 84-87* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/24/04,6/14/04*; 10/12/04; 04/21/05, 05/04/05
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election of Invention of Embodiment of Figures 15-19, claims 17-20, 24, 26-33, 35, 38-77, 80-82 and 84-87 in the reply filed on 04/21/05 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Applicant's election without traverse of Invention of Embodiment of Figures 15-19, claims 17-20, 24, 26-33, 35, 38-77, 80-82 and 84-87 in the reply filed on 04/21/05 is acknowledged.

Claims 21-23, 25, 34, 36, 37, 78, 79, 83, 88-103 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 04/21/05.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 41-43 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 41, it is unclear as to independent claim 17 does not recited any gate electrode and spacers.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 17, 18, 20, 24, 26-33, 35, 38-43, 48, 50-61, 66-71, 74-77, 81, 82 are rejected under 35 U.S.C. 102(e) as being anticipated by Chen et al. (PN 6891,192).

Chen et al. discloses, as shown in Figures 1-18, a method of forming a semiconductor chip, the method comprising:

providing a semiconductor substrate (18,14) comprising a first semiconductor material with a first natural lattice constant;

forming first and second active regions in the semiconductor region

forming a gate stack (25) over the second active region;

forming a masking layer (58) over the first active region;

after forming the masking layer, forming at least one recess (60) in a portion of the second active region not covered by the gate stack;

growing a second semiconductor material (62) in the at least one recess, the second semiconductor material having a second natural lattice constant that is different than the first natural lattice constant;

forming source and drain regions in the second active region to form a first strained channel transistor;

removing the masking layer;

forming a semiconductor component (45) in the first active region.

Regarding claim 18, Chen et al. discloses the step of forming first and second active regions comprises the steps of:

forming trenches (17) to define the active regions;

filling the trenches with a trench filling material;

doping the active regions.

Regarding claim 20, Chen et al. discloses forming the second semiconductor material comprises performing a selective epitaxy step.

Regarding claim 24, Chen et al. discloses forming the source and drain regions comprises performing an ion implantation step.

Regarding claim 26, Chen et al. discloses the gate stack comprises a gate electrode (26) overlying a gate dielectric (13).

Regarding claim 27, Chen et al. discloses the gate stack further comprises a gate mask (52) overlying the gate electrode.

Regarding claim 28, Chen et al. discloses the second natural lattice constant is larger than the first natural lattice constant.

Regarding claim 29, Chen et al. discloses the first semiconductor material comprises silicon and the second semiconductor material comprises silicon and germanium.

Regarding claim 30, Chen et al. discloses forming source and drain regions comprises P-typed doped regions.

Regarding claim 31, Chen et al. discloses the second natural lattice constant is smaller than the first natural lattice constant.

Regarding claim 32, Chen et al. discloses the first semiconductor material comprises silicon and the second semiconductor material comprises silicon and carbon.

Regarding claim 33, Chen et al. discloses the method further comprising a step of forming silicide on the gate stack, the source region, and the drain region of the strained channel transistor.

Regarding claim 35, Chen et al. discloses the semiconductor component comprises a transistor.

Regarding claim 38, Chen et al. discloses the method further comprising:

forming a disposable film over the second active region, the disposable film overlying the gate stack;

processing the disposable film to form disposable spacers on sidewalls of the gate stack in the second active region;

wherein the at least one recess is formed adjacent a disposable spacer.

Regarding claim 39, Chen et al. discloses the method further comprising removing the disposable spacers, and forming spacers on the sidewalls of gate stack.

Regarding claim 40, Chen et al. discloses forming semiconductor component comprising forming a second gate stack over the first active region, wherein the first gate stack and second gate stack each comprises a gate electrode overlying a gate dielectric.

Regarding claim 41, Chen et al. discloses the hard mask over the gate stack.

Regarding claim 42, Chen et al. discloses the hard mask comprises multiple layers of material.

Regarding claim 43, Chen et al. discloses the method further comprising, after growing the second semiconductor material, removing the hard mask.

Regarding claim 48, Chen et al. discloses the method further comprising, after forming the source and drain regions, forming a fist conductive material on the source and drain regions.

Regarding claim 50, Chen et al. discloses, as shown in Figures 1-18, a method of forming a semiconductor device, the method comprising:

providing a semiconductor substrate (18,14) comprising a first semiconductor material, the substrate including a first active region and a second active region, the first active region having a first gate stack (25) formed thereon and the second active region having a second gate stack (45) formed thereon;

forming a film over first active region and second active region;

forming spacers (29) on sidewalls of the second gate stack in the second active region;

etching a source recess and a drain recess (60) on opposing sides of the second gate stack, the source recess and the drain recess spaced from the channel region by the spacers;

growing a second semiconductor material (62) in the source recess and the drain recess.

Regarding claim 51, Chen et al. discloses the first gate stack and second gate stack each comprise a gate electrode (26,42) overlying a gate dielectric (13).

Regarding claim 52, Chen et al. discloses the method further comprising a hard mask overlying the gate electrode.

Regarding claim 53, Chen et al. discloses the hard mask comprises multiple layers (upper portion and lower portion of the masking layer) of hard mask material.

Regarding claim 54, Chen et al. discloses the hard mask comprises silicon oxide (oxide from a TEOS, BSG, ASG, PSG, BPSG).

Regarding claim 55, Chen et al. discloses the method further comprising, after growing the second semiconductor material, removing the hard mask.

Regarding claims 56 and 61, Chen et al. discloses the first semiconductor material comprises silicon.

Regarding claim 57, Chen et al. discloses the second semiconductor material comprises silicon and germanium.

Regarding claim 58, Chen et al. discloses the second semiconductor material comprises silicon and carbon.

Regarding claim 59, Chen et al. discloses the semiconductor substrate comprises an insulator layer (18) underlying the first semiconductor material.

Regarding claim 60, Chen et al. discloses the semiconductor substrate comprises a relaxed SiGe layer underlying the first semiconductor material.

Regarding claim 66, Chen et al. discloses the method further comprising:

forming a first source region and a first drain region in the first active region oppositely adjacent to the firs gate stack;

forming a second source region and a second drain region in the second active region oppositely adjacent to the second gate stack.

Regarding claim 67, Chen et al. discloses the method further comprising, after forming the first source region and the first drain region, forming a first conductive material on the first source region and the first drain region.

Regarding claim 68, Chen et al. discloses the first conductive material comprises cobalt silicide CoSi.

Regarding claim 69, Chen et al. discloses the method further comprising, after forming the second source region and the second drain region, forming a second conductive material on the second source region and the second drain region (not shown, Col. 4, lines 6-12).

Regarding claim 70, Chen et al. discloses the second conductive material comprises cobalt silicide CoSi.

Regarding claim 71, Chen et al. discloses forming spacer on sidewalls of the second gate stack comprises:.

forming a disposable film over the second active region including the second gate stack; forming disposable spacers by etching the disposable film.

Regarding claim 74, Chen et al. discloses the method further comprising removing the disposable spacers after forming the source recess and the drain recess.

Regarding claim 75, Chen et al. discloses the method further comprising, after growing the second semiconductor material, forming spacers on sidewalls of the first gate stack and the second gate stack.

Regarding claim 76, Chen et al. discloses the spacers on the sides of first and second gate staks are composite spacers.

Regarding claim 77, Chen et al. discloses growing a second semiconductor material comprises a performing selective epitaxy process.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 19, 44-47, 49, 62-65, 72, 73, 80 and 84-87 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (PN 6,891,192).

Regarding claim 19, Chen et al. discloses the claimed invention including the method of forming the semiconductor chip as explained in the rejection above. Chen et al. does not disclose forming the second semiconductor material comprises performing a chemical vapor deposition step. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the second semiconductor material of Chen et al. by performing a chemical vapor deposition step because this technique is commonly used to form the semiconductor layer.

Regarding claims 44-47, 62-65 and 80, Chen et al. discloses the claimed invention including the method of forming the semiconductor chip as explained in the rejection above. Chen et al. does not disclose the material of the second semiconductor material or a gate dielectric. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the second semiconductor material of Chen et al. having the materials as that claimed by Applicant, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

Regarding claim 49, Chen et al. discloses the claimed invention including the method of forming the semiconductor chip as explained in the rejection above. Chen et al. further discloses the first conductive material comprises cobalt silicide. Chen et al. does not disclose the material of the first conductive material. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the first conductive material of Chen et al. having the materials as that claimed by Applicant, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

Regarding claim 72, Chen et al. discloses the claimed invention including the method of forming the semiconductor chip as explained in the rejection above. Chen et al. further discloses forming a disposable film and etch the disposable film to form the disposable spacer. Chen et al. does not disclose a masking layer over a portion of the disposable film. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a masking layer over a portion of the disposable film in order to etch the layer underneath the masking layer.

Regarding claim 73, Chen et al. discloses the claimed invention including the method of forming the semiconductor chip as explained in the rejection above. Chen et al. further discloses forming the disposable by etching. Chen et al. does not disclose etching comprises performing a plasma etch process or a wet etch process. However, it would have been obvious to one of ordinary skill

in the art at the time the invention was made to perform the etching by a plasma etch process or a wet etch process because this technique is commonly used to etch the dielectric layer.

Regarding claim 84, Chen et al. discloses the claimed invention including the method of forming the semiconductor chip as explained in the rejection above. Chen et al. further discloses forming second spacers adjacent the second gate stack. Chen et al. does not disclose a step of forming a second masking layer over the first active region and etching the dielectric layer over the second active region to form second spacers adjacent the second gate stack. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a second masking layer over the first active region and etching the dielectric layer over the second active region to form second spacers since this technique is commonly used to form the spacers.

Regarding claim 85, Chen et al. discloses implanting a source region and a drain region comprises implanting a source region and a drain region in the second active region aligned with the second spacers.

Regarding claim 86, Chen et al. discloses the method further comprising, after implanting the source region and the drain region, removing the disposable spacers and the second spacers.

Regarding claim 87, Chen et al. discloses the claimed invention including the method of forming the semiconductor chip as explained in the rejection above. Chen et al. does not disclose forming the lightly doped regions adjacent the gate stacks. However, it would have been

obvious to one of ordinary skill in the art at the time the invention was made to form the lightly doped regions adjacent the gate stacks in order to reduce the hot carrier effect and to improve the performance of the transistors.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung K. Vu whose telephone number is (571) 272-1666. The examiner can normally be reached on Mon-Thurs 6:00-3:30, alternate Friday 7:00-3:30, Eastern Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (571) 272-1732. The Central Fax Number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Vu

July 7, 2005

Hung Vu

Primary Examiner